Chapter 4: Combinational Logic
Solutions to Problems: [1, 5, 9, 12, 23, 30]

Problem: 4-1

Consider the combinational circuit shown in Fig. P4-1.

(a) Derive the Boolean expressions for T_1 through T_4. Evaluate the outputs of F_1 and F_2 as a function of the four inputs.
(b) List the truth table with 16 binary combinations of the four inputs variables. Then list the binary values for T_1 through T_4 and outputs F_1 and F_2 in the table.
(c) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).

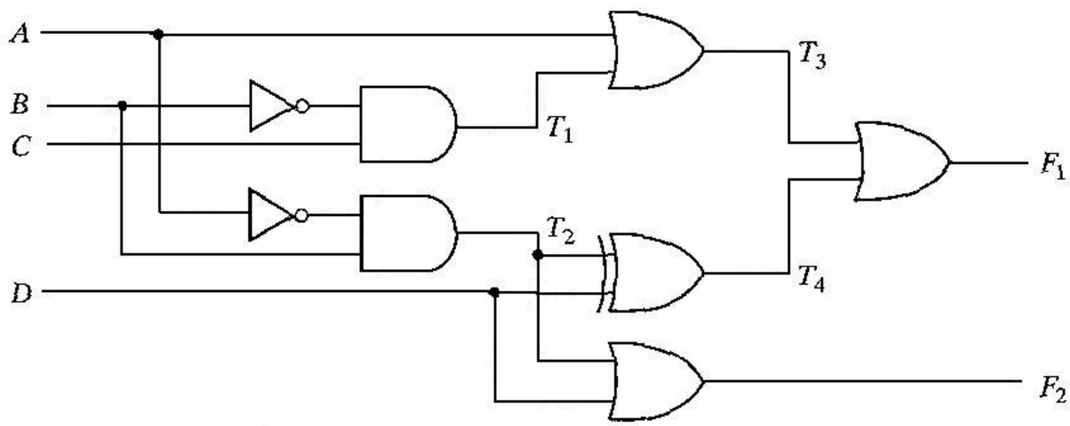


FIGURE P4-1

Solution:

(a) The Boolean expressions for T_1 through T_4. The outputs of F_1 and F_2 as a function of the four inputs.

$$T_1 = B'C \quad T_2 = A'B \quad T_3 = A + T_1 = A + B'C$$

$$T_4 = T_2 \oplus D = A'BD' + (A'B)'D = A'BD' + (A + B')D = A'BD' + AD + B'D$$

$$\begin{aligned} F_1 = T_3 + T_4 &= A + AD + A'BD' + B'C + B'D \\ &= A(1 + D) + A'BD' + B'C + B'D \\ &= (A + A')(A + BD') + B'C + B'D \\ &= A + BD' + B'C + B'D \end{aligned}$$

$$F_2 = D + T_2 = D + A'B$$

(b) The truth table with 16 binary combinations of the four inputs variables with the binary values for T_1 through T_4 and outputs F_1 and F_2:

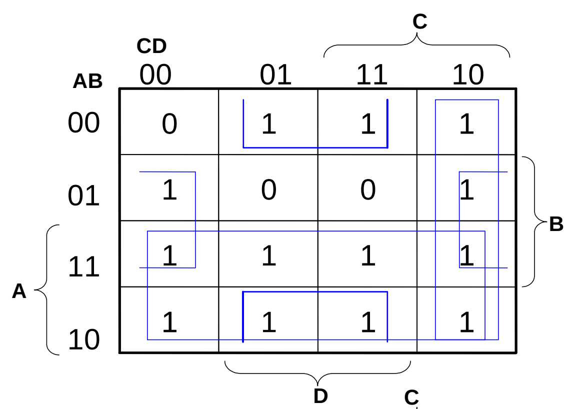
A	B	C	D	T_1	T_2	T_3	T_4	F_1	F_2
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1	1
0	0	1	0	1	0	1	0	1	0
0	0	1	1	1	0	1	1	1	1
0	1	0	0	0	1	0	1	1	1
0	1	0	1	0	1	0	0	0	1
0	1	1	0	0	1	0	1	1	1
0	1	1	1	0	1	0	0	0	1
1	0	0	0	0	0	1	0	1	0
1	0	0	1	0	0	1	1	1	1
1	0	1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1	1	1
1	1	0	0	0	0	1	0	1	0
1	1	0	1	0	0	1	1	1	1
1	1	1	0	0	0	1	0	1	0
1	1	1	1	0	0	1	1	1	1

(c) Plot of the output Boolean functions obtained in part (b) on maps

Map for F_1:

The simplified expression from the map is:

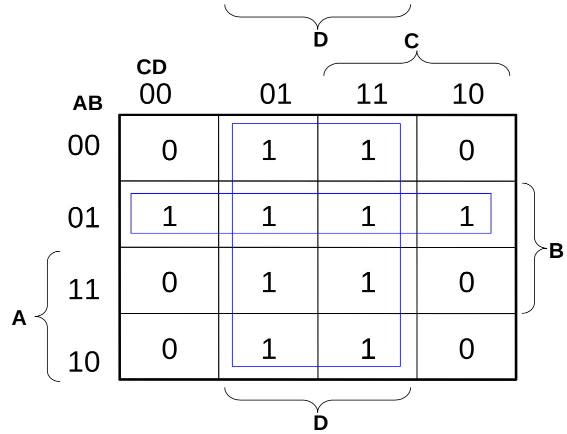
$$F_1 = A + BC + BD' + B'D$$



Map for F_2:

The simplified expression from the map is:

$$F_2 = D + A'B$$



The simplified Boolean expressions are equivalent to the ones obtained in part (a).

Problem: 4-5

Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

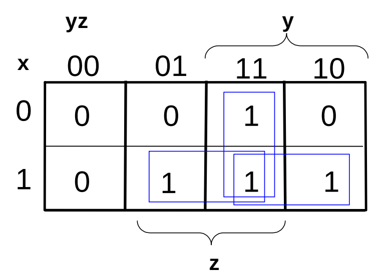
Solution:
Design procedure:

1. Derive the truth table that defines the required relationship between inputs and outputs.

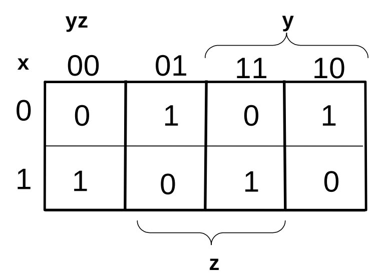
X	Y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

2. Obtain the simplified Boolean functions for each output as a function of the input variables.

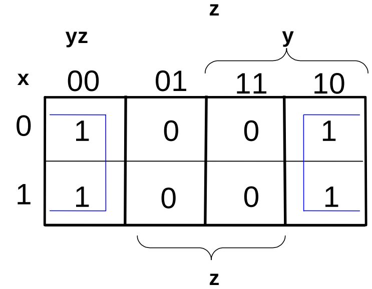
Map for output A:
The simplified expression from the map is:
$A = xz + xy + yz$



Map for output B:
The simplified expression from the map is:
$B = x'y'z + x'yz' + xy'z' + xyz$

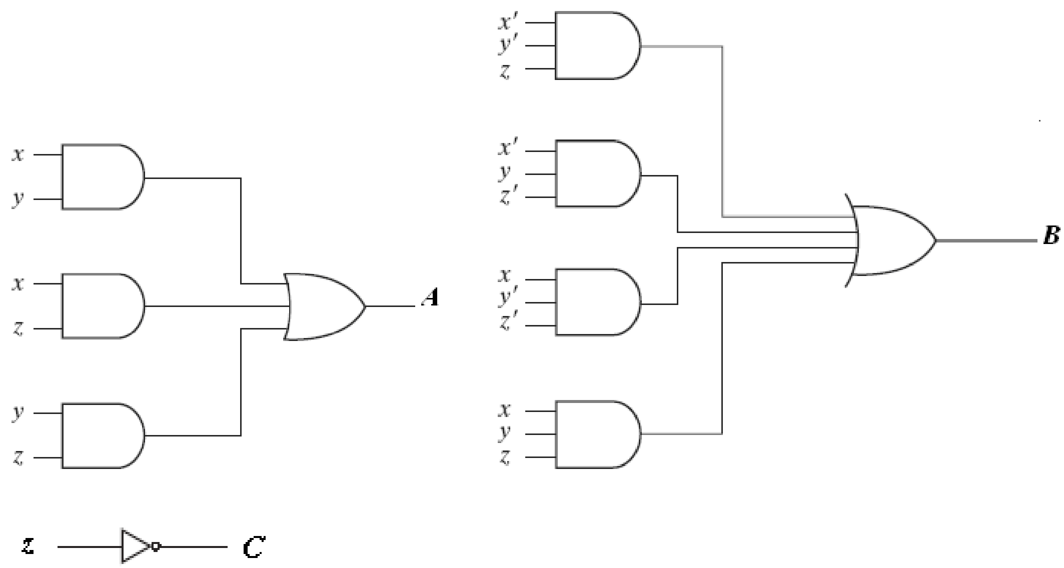


Map for output C:
The simplified expression from the map is:
$C = z'$

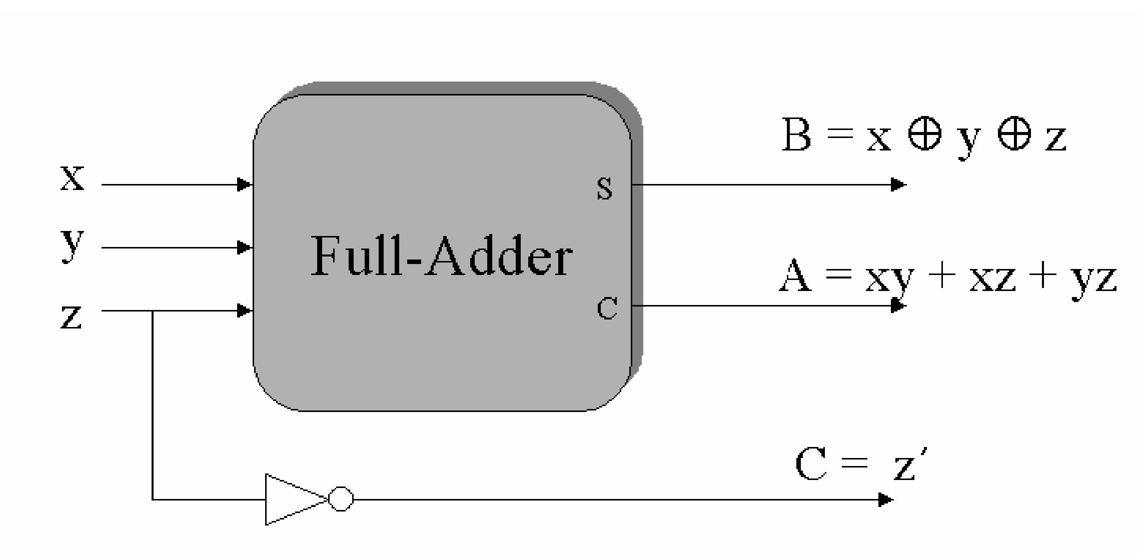


3. Draw the logic diagram.

$A = xy + xz + yz$
$B = x'y'z + x'yz' + xy'z' + xyz$
$C = z'$

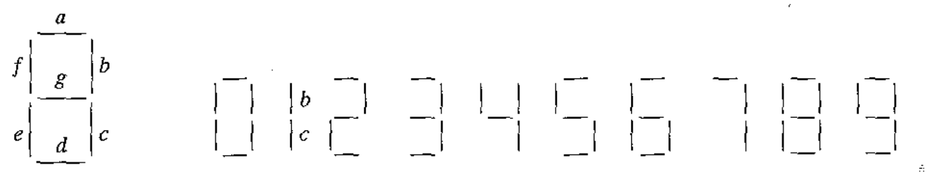


Or alternatively:



Problem: 4-9

A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in a display indicator used for displaying the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display as shown in Fig. P4-9(a). The numeric display chosen to represent the decimal digit is shown Fig. P4-9(b). Design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display.



(a) Segment designation (b) Numerical designation for display

FIGURE P4-9

Solution:

Design procedure:

1. Derive the truth table that defines the required relationship between inputs and outputs.

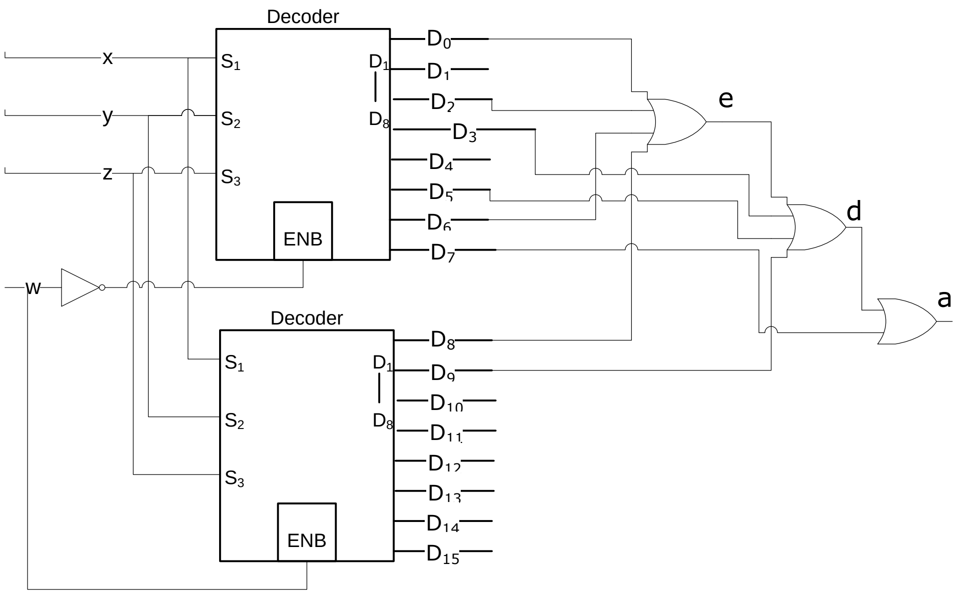
w	x	y	z	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	X	0	0	0	0	0	0	0
1	1	X	X	0	0	0	0	0	0	0

2. Express the Boolean expressions for the outputs (a-g) in sum of minterms

a(w,x,y,z)=$\sum$(0,2,3,5,6,7,8,9)
b(w,x,y,z)=$\sum$(0,1,2,3,4,7,8,9)
c(w,x,y,z)=$\sum$ (0,1,3,4,5,6,7,8,9)
d(w,x,y,z)=$\sum$(0,2,3,5,6,8,9)
e(w,x,y,z)=$\sum$(0,2,6,8)
f(w,x,y,z)=$\sum$(0,4,5,6,8,9)
g(w,x,y,z)=$\sum$(2,3,4,5,6,8,9)

3. Draw the logic circuit. Two 3-to-8-line decoders with enable inputs have been connected to form a 4-to-16-line decoder. Together they generate all the minterms of the input variables. OR gates are to be used to implement each of the functions a-g. The inputs to each OR gate are selected from the decoder outputs according to the list of minterm of each function.

The diagram below shows the circuit for output a, d and e. The same procedure should be followed to include the remaining functions and complete the logic circuit.



Problem: 4-12

(a) Design a half subtractor circuit with inputs x and y and outputs D and B. The circuit subtracts the bits x-y and places the difference in D and the borrow in B.

(b) Design a full subtractor circuit with three inputs x, y and z and two outputs D and B. The circuit subtracts the bits x-y-z, where z is the input borrow, B is the output borrow and D is the difference.

Solution

(a) To design a half subtractor circuit with inputs x and y and outputs D and B. The circuit subtracts the bits x-y and places the difference in D and the borrow in B.

Design procedure:

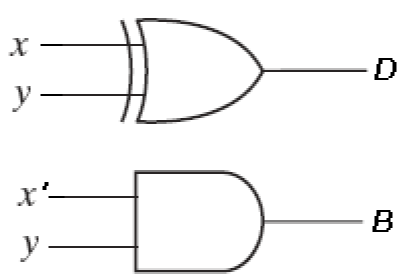
1. Derive the truth table that defines the required relationship between inputs and outputs.

x	y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

2. Obtain the simplified Boolean functions for each output as a function of the input variables.

D=x’y+xy’
B=x’y

3. Draw the logic diagram.



Solution

(b) Design a full subtractor circuit with three inputs x, y and z and two outputs D and B. The circuit subtracts the bits x-y-z, where z is the input borrow, B is the output borrow and D is the difference.

Design procedure:

1. Derive the truth table that defines the required relationship between inputs and outputs.

x	y	z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

2. Obtain the simplified Boolean functions for each output as a function of the input variables.

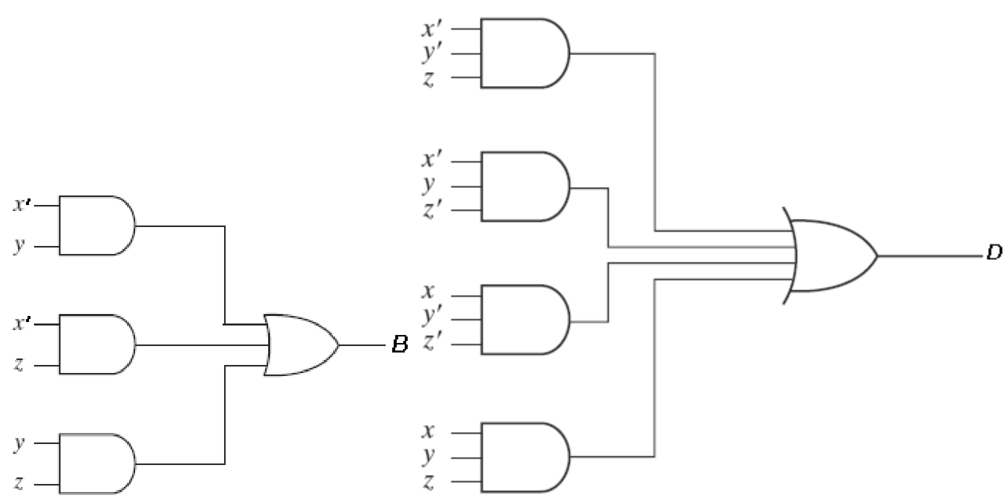
x \ yz	00	01	11	10
0	0	1	0	1
1	1	0	1	0

D=x'y'z+x'yz'+xy'z'+xyz

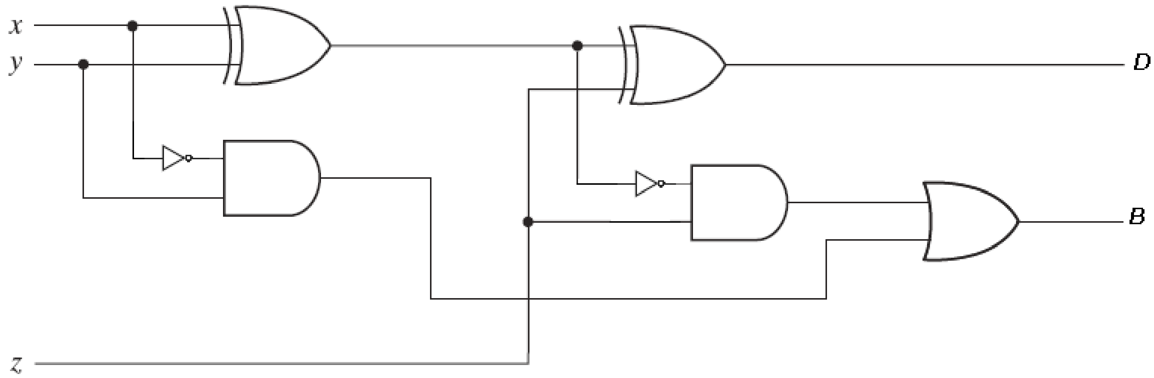
x \ yz	00	01	11	10
0	0	1	1	1
1	0	0	1	0

B=yz+x'y+x'z

3. Draw the logic diagram.



Or alternatively using 2 half subtractor and an OR gate:



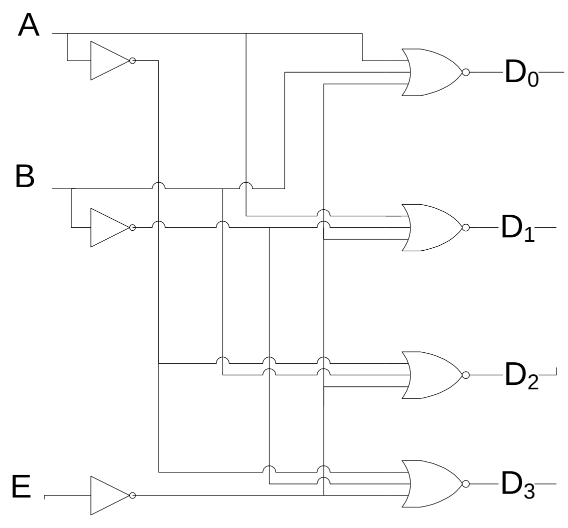
Problem: 4-23
Draw the logic diagram of a 2-to-4 line decoder using NOR gates only. Include an enable input.

Solution:
Design procedure:
1. The truth table for the circuit.

E	A	B	D_0	D_1	D_2	D_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

$D_0 = EA'B' = (E'+A+B)'$ $D_1 = EA'B = (E'+A+B')'$
$D_2 = EAB' = (E'+A'+B)'$ $D_3 = EAB = (E'+A'+B')'$

2. The logic diagram



Problem: 4-30
Specify the truth table of an octal to binary priority encoder. Provide an output V to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four inputs if inputs D_5 and D_3 are 1 at the same time?

Solution:
Below is the truth table of an Octal-to-Binary priority encoder with an output V to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z	V
0	0	0	0	0	0	0	0	X	X	X	0
1	0	0	0	0	0	0	0	0	0	0	1
X	1	0	0	0	0	0	0	0	0	1	1
X	X	1	0	0	0	0	0	0	1	0	1
X	X	X	1	0	0	0	0	0	1	1	1
X	X	X	X	1	0	0	0	1	0	0	1
X	X	X	X	X	1	0	0	1	0	1	1
X	X	X	X	X	X	1	0	1	1	0	1
X	X	X	X	X	X	X	1	1	1	1	1

The value of the four outputs if inputs D_5 and D_3 are 1 at the same time will be X=1, Y=0, Z=1, V=1.